Sr. No. 018403

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B.Tech. (CSE(AIML)/ CE/ CSE/ IT)- IV SEMESTER

Computer Organization and Architecture (PCC-CS-402)

Time: 3 Hours **Max. Marks:75**

Instructions:
1. *It is compulsory to answer all the questions (1.5 marks each) of Part -A in short.*
2. *Answer any four questions from Part -B in detail.*
3. *Different sub-parts of a question are to be attempted adjacent to each other.*

PART -A

Q1 (a) Mention the register transfer statements used to represent the conditional control statement: **If (P=1) then (R1←R2) else if (Q=1) then (R1←R3)** (1.5)

(b) Where is the Booth multiplication Algorithm used? (1.5)

(c) List 4 peripherals that produce an acceptable output for a person to understand. (1.5)

(d) Explain the memory operation in the register transfer statement: **M[AR]←R3** (1.5)

(e) Given a number N in base r, What is *r* complement and ***(r-1)*** 's complement of N? (1.5)

(f) What are the four different commands that an interface may receive during synchronization of all input and output transfers with the CPU? (1.5)

(g) What is a three-state buffer? (1.5)

(h) How many characters per second can be transmitted over 1200 baud line in asynchronous serial transmission with one and two stop bits if each character code is of 8 bits? (1.5)

(i) What are the two different cache-write policies? (1.5)

(j) What is a control Function? (1.5)

PART -B

Q2 (a) A computer uses a bus system based on multiplexers and has 16 registers of 32 bits each. (5)
How many multiplexers and selection inputs are needed in each mux to design the bus system? Also what should be the suitable size of the multiplexer?

(b) What is wrong with the following register transfer statements? (6)
a) xT: AR←AR' , AR←0
b) yT: R1←R2 , R1←R3
c) zT: PC ← AR, PC ← PC +1

(c) **Consider R=1101 1101, determine the sequence of binary values in R after logical shift left, followed by circular shift right, followed by logical shift right.** (4)

followed by circular shift left.

Q3 (a) Calculate (-42) +(-13) and (-42)-(-13) in binary using signed 2's complement representation for negative numbers. (6)

(b) What is a partial remainder? Also provide the name of the method and its purpose in arithmetic operations. (4)

(c) **Justify the statement :** " Overflow can't take place when two ***n***-digit numbers in base ***r*** are multiplied together'. (5)

Q4 (a) The main memory of a computer is organized as 64 blocks with a block size of eight words. The cache has eight block frames. Show the direct mapping from the numbered blocks in main memory to the block frames in the cache. Draw all lines showing the mappings as clearly as possible. Also show, the address bits that identify the tag field, the block number, and the word number. (6)

(b) How many 128 * 8 RAM chips are needed to provide a memory capacity of 2048 bytes? How many lines of address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips? How many lines be decoded for chip select? specify the size of decoders. (4)

(c) What are common page-replacement policies used to handle page-faults? (5)

Q5 (a) What are the major differences between a CPU and peripherals that mandate the use of communication link between them? (5)

(b) Explain in detail how data transfer takes place between: (10)
a) the CPU and the interface
b) the interface and the I/O devices

Q6 (a) What is the major benefit offered by different cache organizations? (3)

(b) Describe the different methods by which the miss rate or miss penalties can be minimized. Also throw light on any trade-offs associated with them (7)

(c) Explain different cache organizations (5)

Q7 (a) Differentiate between a hardwired and microprogrammed decoder. (5)

(b) Write short notes on any two: (10)
(a) Type of Interrupts and their role
(b) Parallel and pipelined processors
(c) Memory interleaving.

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